VFO and Buffer-Amplifier for Johnson Viking II

F1LAG – January/April 2019

The VFO is a Wavehunter dual channel VFO based on a single BF245C FET. It gives a moderate amplitude signal and has high output impedance.

The Johnson Viking II needs a fairly large input signal at the VFO socket. Here are two extracts from the Johnson Viking II manual:

VFO EXCITATION: The "O" position of the crystal selector switch connects the VFO receptacle at the rear of the chassis directly to the 6AU6 oscillator grid through approximately one foot of RG59U cable. An isolating condenser of 50 to 150 mmfd is necessary between the VFO and Viking II input unless the VFO has a capacity coupled output (the Johnson VFO may be directly coupled). 6 volts of 40 meter RF at the grid of the Viking II 6AU6 oscillator stage will drive the final to full excitation on 10 meters. The lower frequency bands require less VFO output. The VFO frequency range should be nominally the same as the crystal frequencies which would normally be used. There is a danger of overdriving the 6AU6 with a VFO resulting in grid blocking. Grid blocking actually reduces the effectiveness of the stage to the point where it attenuates the input signal greatly rather than passing or amplifying the input signal or generating the required harmonics.

Use the VFO in the same manner as crystals are used for output on the band selected. Only two volts of 160 meter signal at the Viking II 6AU6 grid will drive the transmitter to full output on 160 to 80 meters. The 160 meter VFO signal will also drive 40 meters satisfactorily. Six volts of 40 meter VFO excitation at the 6AU6 grid will be sufficient to drive the Viking II to full output on all bands, 40 meters through 10 meters. The R.F. Voltage at the 6AU6 grid should be limited to a value of less than 15 to 20 volts to prevent the stage from blocking.

The 'Assembly and Operation Instruction Manual' of the Johnson Viking VFO provides the following information:

C. Operation

1. General Operating Characteristics and Requirements

a. The Viking Model 122 VFO has been designed as a crystal substitute The output of

a minimum of 8 volts r.m.s. across 25,000 ohms in the frequency range of 7.00 to 7.425 mc and
a minimum of 5.5 volts r.m.s. across 25,000 ohms in the frequency range of 1.75 to 2.00 mc

may be applied across the crystal oscillator grid circuit of many transmitters directly, to take the place of 160 meter and 40 meter crystals normally used with the transmitters. A recommended basic transmitter first stage oscillator-amplifier circuit and a recommended booster amplifier will be discussed later for transmitters where more VFO isolation or output is required.

Therefore the Wavehunter VFO must be followed by a buffer-amplifier. Based on the above Johnson information and taking some margin, its output capability for the 40m band should be:

- Minimum: 6 V rms (17 Vpp)
- Target: 8 to 12 V rms (23 to 34 Vpp)
- Maximum: 15 V rms (42 Vpp)
- Load impedance: 25 kΩ

Wavehunter VFO

Preliminary tests

Assembly of the VFO kit and first tests were done by F6HOY. An initial measurement gave about 200 mVpp both on 3.628MHz and 7.1907 MHz. Further tests in different configurations have been done: with or without connection to the frequency meter, without any load or with a 1 kΩ resistor either in series or across the VFO output.

Output (mVpp)	No load	1kΩ load	1kΩ series	With FX no load	With FX 1kΩ series
80m	320	240	200	100	90
40m	110	100	50	40	40

The output impedance of the VFO and the input impedance of the measuring device (probe and oscilloscope) can be calculated from these measurements (see Appendix). However this only a theoretical approach as it assumes purely resistive loads and that the circuit behavior is not influenced by the load. This is probably far from reality for the VFO and the results are just very approximate. Nevertheless, the results are strange as it would indicate a much too low oscilloscope impedance (it should be in the MΩ range).

	Zout VFO	Zin oscillo
80m	460 Ω	1206 Ω
40m	116 Ω	717 Ω

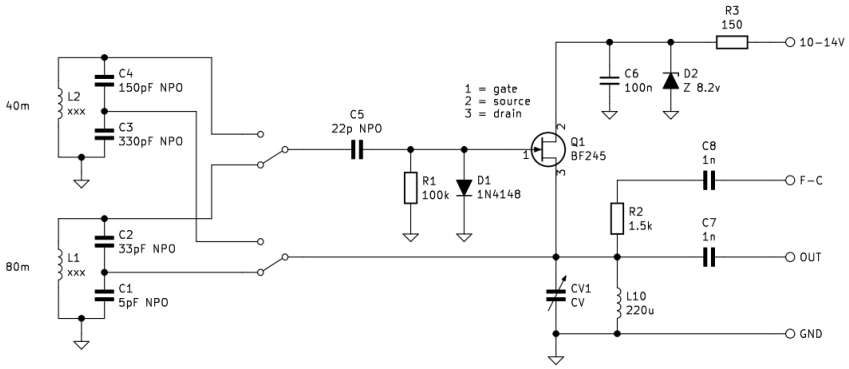
Another problem with F6HOY tests is that now the frequency could not be raised above 3.2 MHz although the first test gave 3.628MHz. Also, the output amplitude is much smaller than what the Wavehunter website shows (3 Vpp on 80m, 1.55 Vpp on 40m). A second VFO kit had the same issue of the 80m output which could not go higher than 3.2 MHz even with a different power supply.

The reasons for these bad results are still a total mystery!

F6HOY send me one of the VFO kits for further investigations.

A second look at the VFO

I first redraw the VFO schematic from the Wavehunter website documentation. With other FET VFO circuits I found, the FET has its drain on the supply side and its source on the HF output side. The Wavehunter circuit has reversed drain and source connections. In fact it does not matter: the BF245 FET is fully symmetrical (this is also true for the J309-J310 FETs).

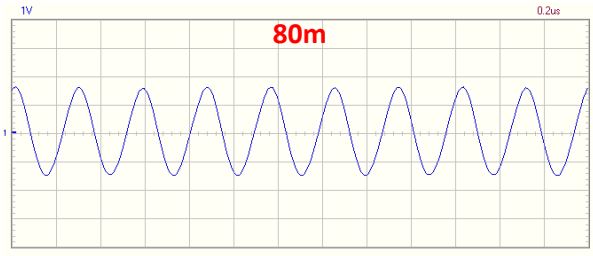


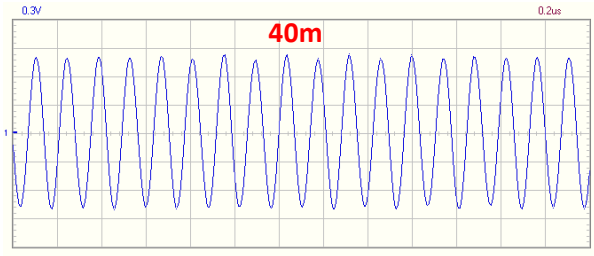
Wavehunter 2-band VFO

First observations after I received the VFO: following F6HOY tests C3 330pF is missing, C1 and C2 are on the bottom side of the PCB. The other components are checked with a PEAK LCR45 tester: all have the correct values except C8 which is a 150pF capacitor instead of 1nF.

Test of the VFO are carried out with a KA3005P laboratory power supply, a Velleman PCSU200 oscilloscope plus Conrad C3000 probe and a small pick-up coil connected to an RTL-SDR to check the frequency.

After reinstalling C3, the VFO is tested (probe in x10 position, oscilloscope display in x10 position i.e. it shows the actual amplitude). I get 3.472 MHz 3.10 Vpp on 80m and 7.072 MHz 1.65 Vpp on 40m. This first test is successful: the amplitude is the same as what the Wavehunter website shows and the frequency is correct.



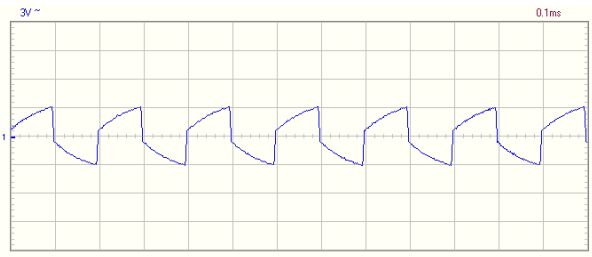


Next, the frequency span is checked between the min and max positions of the CV. Leaving the 40m L2 coil in its position, the output frequency goes from 7.080 MHz to 7.205 MHz, a 125 kHz span. On 80m, the measurement is done for different adjustments of the L1 coil:

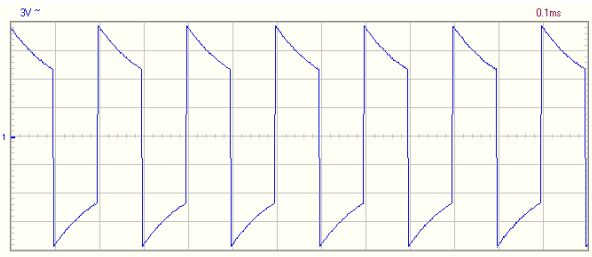
	F min	F max	F span
L1 min	3.645 MHz	4.050 MHz	405 kHz
L1 adjusted	3.493 MHz	3.887 MHz	394 kHz
L1 max	2.531 MHz	2.864 MHz	333 kHz

Before going further, C1 and C2 needed to be put back to the top side of the PCB. C2 was checked ok at 5.8 pF. C1 was marked 33pF but measured as 48 pF; also the coating resin was cracked. It is replaced with a 33 pF (but an X7R type, I do not have any 33 pF NPO). Obviously the frequency changes but also the available span. After readjusting L1, the frequency range becomes 3.498-3.787 MHz, a 290 kHz span when previously it was 390 kHz.

Next, two series of tests are done to check the effect of various loadings at the VFO output. The first series consists in testing the probe impact: x1 position, x10 position under compensated or compensated or over compensated. The probe compensation is essential to get a proper amplitude reading and to prevent capacitive loading of the tested circuit. The following oscilloscope displays are for the *same perfect* 5 kHz square signal when the probe is under or over compensated: a huge difference!



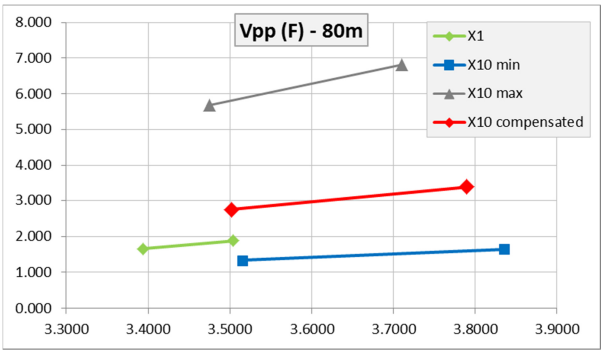
Under compensated (x10 min)

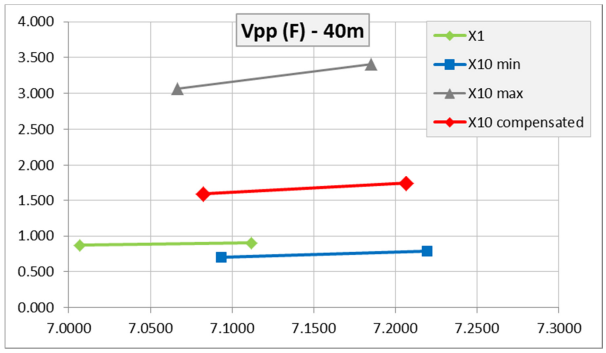


Over compensated (x10 max)

The following table and graphs give the results obtained at the VFO output with the various probe setups. In the x1 position there is a significant capacitive loading which lowers the frequency and reduces the frequency span. The impact is obviously larger on the 80m band where the VFO capacitors across the coil are smaller. In the x10 position, the capacitive loading in the under and over compensated cases are less than in the x1 position but still present. The impact on the amplitude reading is very large (a factor x4 between the over and under compensated cases). This illustrate the importance of a proper probe compensation but cannot fully explain the strange results obtained in F6HOY's testing.

	80m				40m			
Probe	F min	F max	Vpp	Vpp	F min	F max	Vpp	Vpp
X1	3.3940	3.5044	1.653	1.878	7.0070	7.1120	0.869	0.903
X10 min	3.5155	3.8357	1.341	1.650	7.0930	7.2190	0.703	0.788
X10 max	3.4755	3.7105	5.688	6.813	7.0665	7.1850	3.063	3.406
X10 compensated	3.5020	3.7898	2.750	3.375	7.0825	7.2065	1.584	1.734
No probe	3.5600	3.9735	n/a	n/a	7.1160	7.2470	n/a	n/a





The next series of tests are done with a properly compensated probe in the x10 position and with different loads connected across the VFO output and ground: no load (apart from the probe, obviously), 10 kΩ resistor or 1 kΩ resistor.

	80m				40m			
Load	F min	F max	Vpp	Vpp	F min	F max	Vpp	Vpp
No load	3.500	3.790	2.719	3.344	7.083	7.209	1.594	1.734
10 kΩ	3.503	3.795	2.531	3.125	7.085	7.211	1.566	1.772
1 kΩ	3.538	3.895	1.931	2.184	7.091	7.215	1.322	1.416

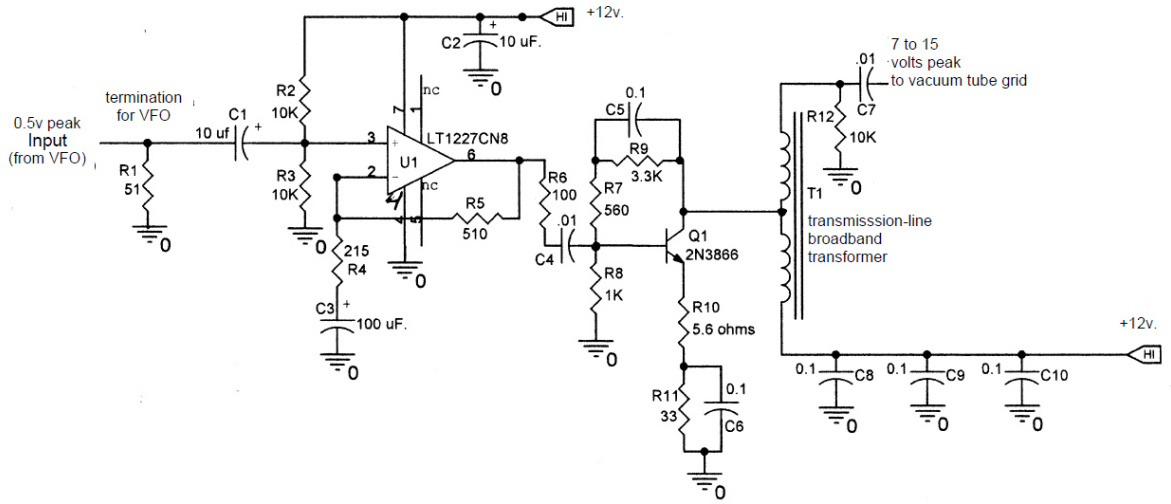
The 10 kΩ load has little effect in terms of frequency and moderate impact on the output amplitude. As expected, the 1 kΩ load has a larger effect on the output amplitude but it also significantly impacts the higher frequency limit on the 80m band.

The VFO consumption was also measured at 23 mA.

Finally, this little VFO is working as it should.

Buffer-Amplifier Options

For the buffer-amplifier, I found a good paper by WA1FFL (*An Improved VFO Driver for Tubes Rigs – CQ June 2011*). The final amplifier stage uses a single 2N3866 NPN transistor; this is the circuit that I will reuse. The first stage uses a video AOP LT1227. It brings some voltage gain (about x1.8). However, I do not have any video AOP available. Therefore, a different solution must be found. From the VFO test it was established that the input impedance of the first buffer stage should be in the 10 kΩ range. We need to estimate its target output impedance. This is done by modeling the 2N3866 amplifier stage with LTSpice software.



WA1FFL buffer-amplifier

Analysis of WA1FFL amplifier stage with LTSpice

The 2N3866 spice model is available from various libraries. But we first need to build a model for the transformer.

FT50-43 transformer model

The transformer is made of a 10 turn's bifilar winding on FT50-43 tore. Permeability of ferrite material 43 depends on frequency and it presents a significant resistive component. Based on the FairRite permeability curves, the following values have been calculated:

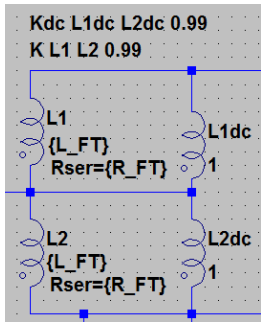
	Rs	L
200 kHz	0.5Ω	43 µH
3.6 MHz	278 Ω	26 µH
7.1 MHz	560 Ω	18 µH

Measured values with a PEAK LCR45 tester are 39 µH and 0.05Ω at 200 kHz. Considering the fairly large tolerance of the material specification, this is close enough to the calculated values.

The transformer is simply modelled as two coupled inductors but the inductance and series resistance values need to depend on the frequency. As the simulation will only be used at two frequencies (3.6 MHz and 7.1 MHz), the simplest way is to use a parametric statement with a threshold frequency arbitrarily fixed midway at 5 MHz.

FT50-43 frequency data
at 3.6MHz: L=26u Rs=278
at 7.1MHz: L=18u Rs=560

.param L_FT if(F<5e6,26u,18u)
.param R_FT if(F<5e6,278,560)



As the coil series resistance varies with frequency, the transformer model still needs to be completed for its DC characteristic.

A simple way is to add two very large parallel inductances (1 Henry): they have no influence on the HF behavior and provide a perfect shunt for DC current.

Simulation of WA1FFL amplifier

The simulation is done at two frequencies: 3.6MHz and 7.1MHz. The input point is at C4. A first simulation of WA1FFL amplifier is done with the AC mode of LTSpice to get an estimate of the input and output impedances with a 25 kΩ load. Running the TRAN mode, we get the voltage gain for different loads. These simulations are run with a low input voltage (100 mV peak) to keep clear from saturation or clipping domain.

Input at C4	Z in	Z out	Av - 1kΩ load	Av - 25kΩ load
3.6 MHz	13.8 Ω	1.20 kΩ	33.3	66.2
7.1 MHz	10.9 Ω	1.65 kΩ	30.8	74.3

Running the simulation at different input levels and looking at the FFT results, we see that the second harmonic level is about -40dB for the 100mV low input applied at C4 but it rises to about -20dB or worse when the input level goes higher than about 300mV at 3.6MHz or about 200mV at 7.1MHz.

For a minimum output equal to 6 Vrms (8.5 Vpeak) and a voltage gain of about 70, we need an input signal at C4 equal to 120 mVpeak. The Wavehunter VFO gives a significantly greater signal; however, to maintain this level and prevent overloading, it needs to be connected to a load larger than 10 kΩ. The amplifier input impedance at C4 being only 10 Ω, we need a buffer (voltage follower) in between the VFO and amplifier.

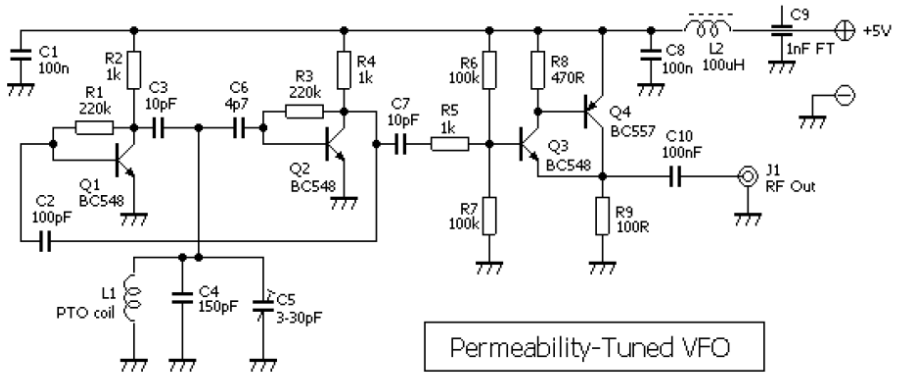
If we chose the input point at R6 instead of C4, then the input impedance is mainly driven by R6 (100 Ω) and the global available voltage gain is reduced because R6 makes a voltage divider with the input impedance previously calculated at C4.

Input at R6	Z in	Z out	Av - 1kΩ load	Av - 25kΩ load
3.6 MHz	110.7 Ω	637 Ω	5.25	8.31
7.1 MHz	109.9 Ω	1005 Ω	3.89	7.43

First buffer stage – ZL2PD circuit

Between the VFO and amplifier we need a voltage follower to adapt the impedance from 10 kΩ to 10 Ω. This is a factor 1000 which cannot be achieved with common emitter circuits using a single transistor (it would need a much too high current gain).

I found a good circuit by ZL2PD (https://www.zl2pd.com/ptovfo.html) aimed at his PTO design (there are plenty of other good circuits at ZL2PD website).



ZL2PD oscillator and buffer

The NPN-PNP (Q3-Q4) arrangement is a Sziklai transistors pair. It is rather like a Darlington arrangement but has some advantages (lower base-emitter voltage drop, more immune to thermal runaways, etc.). In the voltage follower configuration that we use, it gives us a current gain equal to the product of the transistors β (same as with the Darlington pair); therefore, we get the capability to have a high input/output impedance ratio.

LTSpice simulation of ZL2PD voltage follower

The simulation is carried out using BC547B / BC 557B transistors that I have available. The simulation is first run in the AC mode to get the input and output impedances. Running the TRAN mode, we get the voltage gain for a 10 Ω load. These simulations are run with a low input voltage (100 mV peak) to keep clear from saturation or clipping domain.

	Z in	Z out	Av – 10 Ω load
3.6 MHz	9.8 kΩ	0.46 Ω	0.96
7.1 MHz	3.3 kΩ	2.10 Ω	1.06

Running the simulation at different input levels and looking at the FFT results, we see that the second harmonic level is about -40dB for 100mV at 3.6MHz and -35dB for 80mV at 7.1MHz. It rises to about -20dB or worse when the input level goes higher than about 180mV at 3.6MHz or about 150mV at 7.1MHz.

The input impedance depends heavily on the load. For example, input impedance is 6.3kΩ/1.8kΩ when the load is reduced to 5Ω. The output impedance is nearly unchanged.

We see that this circuit can easily provide the impedance adaptation we need between the VFO and the amplifier. The input and output impedances partially depend on the values of the linking components (C7, R5 and C10 in ZL2PD schematic) and on the output load. In the actual implementation we will also need to adjust the bias point for a 12V power supply instead of the original 5V.

F1LAG Buffer-Amplifier

There are a few required adjustments before we go to the final circuit:

- The first stage buffer must be adapted for 12V power supply.
- The amplifier gain needs to be lowered.
- We shall ensure that the harmonic content at the output is low.
- If possible, the amplifier gain should be less on the 80m band to, at least partially, compensate for the VFO output which is twice higher on this band than on the 40m band.

LTSpice simulations

After running multiple LTSpice models of the buffer-amplifier, the following choices are made:

- Adjustment of the first buffer stage for 12V power supply is simple: just change the resistor at Q3 emitter from 100Ω to 330Ω.
- Lowering the amplifier gain is first done by lowering the collector current. This is achieved with higher resistance values at the 2N3866 emitter (47Ω + 47Ω instead of 5.6Ω + 33Ω).
- Lowering the value of the linking capacitor between buffer and amplifier from 100nF down to 470pF achieved two goals. It introduces an impedance which is significant at the working frequency and this makes a voltage divider with the amplifier input impedance; therefore, the global gain is lowered. But the main objective is that this impedance varies with frequency (higher at lower frequency); therefore, it also provides some compensation of the VFO output level which is quite different on 80m and 40m bands.
- Some further level compensation is done by lowering the bypass capacitor at 2N3866 emitter from 100nF down to 10nF.

In addition, the linking capacitor at the buffer entry is changed to 470 pF but this has negligible effect. Also choke inductors are added at the power supply lines. In all these simulations, I did not make much detailed attempts at modifying the biasing at the base of the transistors: the above modifications appeared to be sufficient to achieve the objective.

As previously done, the simulations are run in the AC mode to get the input and output impedances and in the TRAN mode to get the voltage gain and harmonic level. But unlike the initial simulations, the input level is the one

measured at the Wavehunter VFO output so that the actual harmonic level can be estimated (worst case is either the 2nd or 3rd harmonic).

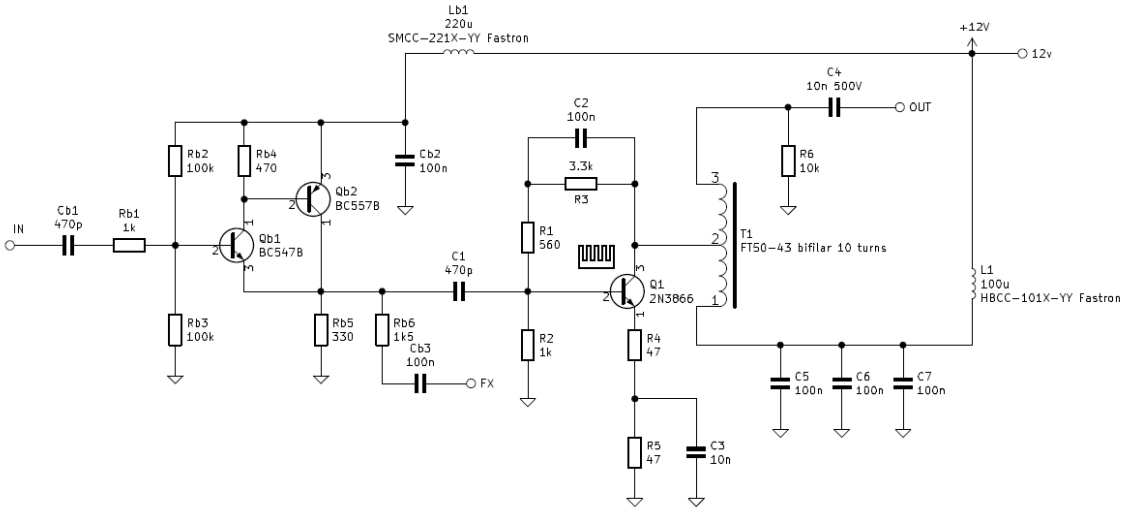
Simulations results are summarized in the following table:

	Input	Z in	Z out	Load = 25 kΩ			Load = 10 kΩ		
				Output	Av	F2 or F3	Output	Av	F2 or F3
3.6 MHz	1.5 V peak	24.7 kΩ	930 Ω	15.5 Vpp	5.18	-39 dB	14.9 Vpp	4.96	-37 dB
7.1 MHz	0.8 V peak	13.2 kΩ	1.43 kΩ	11.8 Vpp	7.39	-46 dB	11.1 Vpp	6.92	-46 dB

When fed through a 10nF capacitor instead of 470pF, the input impedance of the amplifier stage alone is 77Ω / 68Ω. This is to be compared to 13.8 Ω / 10.9 Ω obtained in the initial configuration before the emitter resistance values were modified.

Circuit schematic

Here is the buffer-amplifier circuit following the adjustments based on the above LTSpice simulations (note that components references are changed when compared to original ZL2PD / WA1FFL circuits). I also added an output for connection to a frequency meter after the first buffer stage.

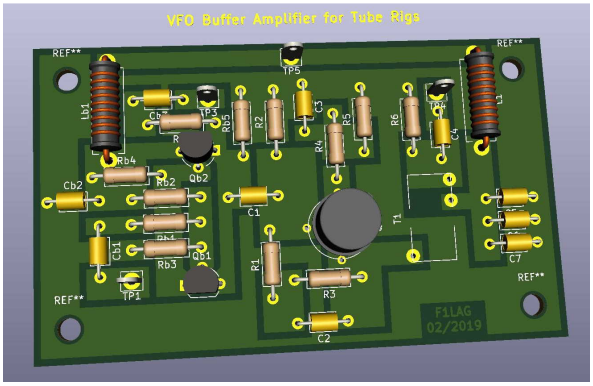


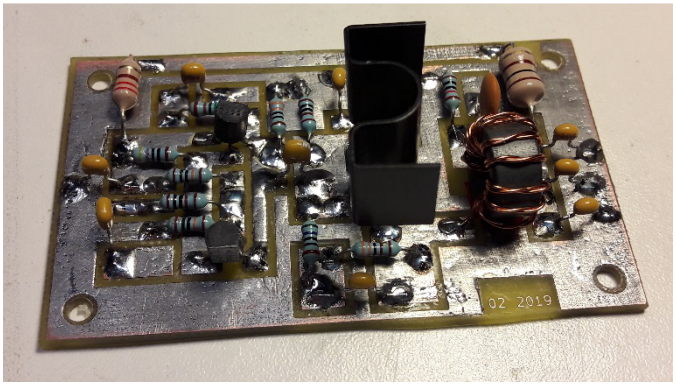
F1LAG buffer-amplifier

However, there was a mistake here. It works but it might not be the final circuit.
More on this at the end of the document…

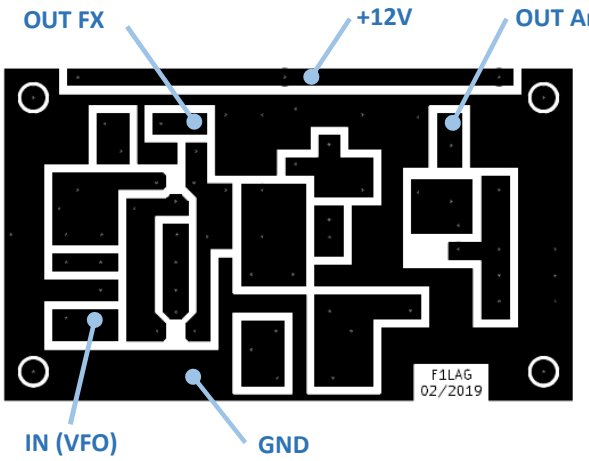
Construction

The buffer-amplifier is implemented on a 77mm x 45mm single sided PCB. The circuit is designed with large copper pads instead of thin traces (minimum etching) and the components are mounted on the copper side. The amplifier transistor is fitted with a small heatsink although it might not be strictly necessary (warning: the 2N3866 case and heatsink are connected to the emitter, thus they are at the power supply rail voltage).



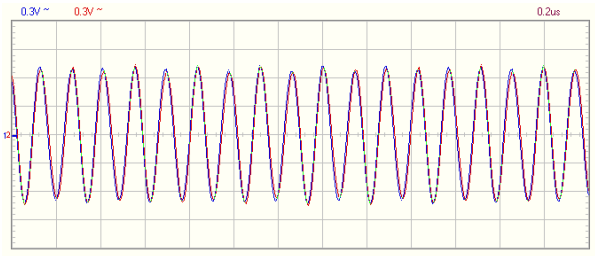


KICAD 3D view and the real thing



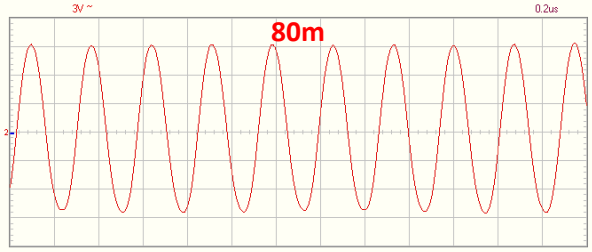
PCB connection pads

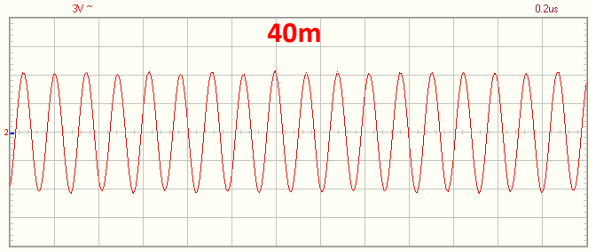
Tests



First test is with the buffer stage alone, i.e. C1 is left unconnected at the amplifier side. The buffer works exactly as expected: a 1 to 1 voltage transfer in this configuration (see figure where the input and output oscilloscope traces are identical).

Next, VFO, buffer and amplifier are connected together, and the full system is tested with a 10kΩ load (Viking target impedance is 25kΩ but 10kΩ was selected to be on the safe side). It gives good results both in terms of output amplitude and signal shape (this is just a visual check, I do not have a proper spectrum analyzer…)





The output amplitude is in fact larger than calculated with LTSpice.

	measured	LTSpice	meas/calc
80m	17.7 Vpp = 6.3 Vrms	14.9 Vpp = 5.3 Vrms	+ 19%
40m	13.0 Vpp = 4.6 Vrms	11.1 Vpp = 3.9 Vrms	+ 17%

There are several potential reasons for this larger amplitude. The actual β of the used transistors might be larger than what is used in the simulation. Also, the series resistance of the inductors in the transformer might be lower than estimated (ferrite specifications have rather large tolerances). Also, we should not forget that LTSpice is not the real world: although very powerful, it is just a theoretical numerical simulation!

It is when writing down the above table that I discovered an error.

The big stupid mistake: during component value adjustment using LTSpice, I wrongly mixed up peak and peak-to-peak voltages! So, I was lowering the amplifier gain to get about 12-15 Vpp, it should have been 12-15V peak!

As it is, the buffer-amplifier might give a bit too low amplitude to properly drive the Viking (the target was 6V rms minimum amplitude). See next chapter for what needs to be done to raise the output level.

The power consumption was also measured:

VFO 23mA
VFO + buffer 30mA
VFO + buffer + amplifier 58mA

Potential future modifications

I ran a new series of LTSpice simulations to define the modifications needed to get a larger output. Just lowering the emitter resistance R4 was not satisfactory as the harmonic content was quickly increased.

The solution is something I had not previously investigated in detail: it consists in changing the values of the base resistors (R1 and R3). This modify the quiescent point and provides more headroom for larger signals before distortion comes in. The selected values are **R1 = 1kΩ** and **R3 = 2.2kΩ.**

Now, the emitter resistor can be lowered without scarifying the harmonic content. The tables below show simulation results for various values of R4 (lower values for higher gain) and an output load equal to 25 kΩ.

With the new values for R1 and R3, the input and output impedance of the buffer-amplifier do not change much. As a side benefit, the second harmonic level is lower on the 80m band than in the initial configuration.

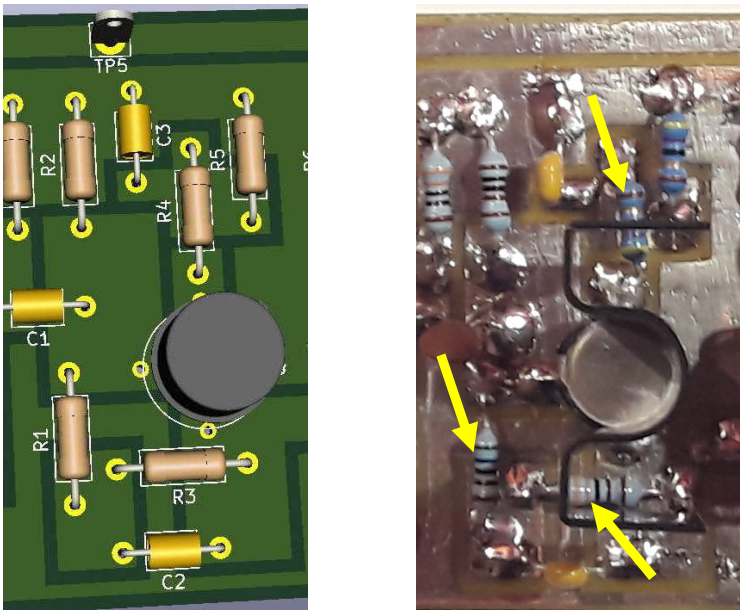
Knowing that the actual output was about 20% larger than calculated, keeping R4 as it was (47Ω) might be acceptable (the minimum required level is 6Vrms), but a 39Ω value is probably better. In any case do not go lower than 27Ω or the harmonic level might quickly degrade (at least this is what LTSpice shows…).

R4 = 47 Ω	Input	Output	Av	F2	Z in	Z out
3.6 MHz	1.5 V peak	8.44 V rms	7.94	-43 dB	24.5 kΩ	1.14 kΩ
7.1 MHz	0.8 V peak	6.34 V rms	11.2	-44 dB	13.1 kΩ	1.70 kΩ

R4 = 39 Ω	Input	Output	Av	F2	Z in	Z out
3.6 MHz	1.5 V peak	9.33 V rms	8.77	-44 dB	24.7 kΩ	1.07 kΩ
7.1 MHz	0.8 V peak	7.25 V rms	12.8	-43 dB	13.3 kΩ	1.64 kΩ

R4 = 33 Ω	Input	Output	Av	F2	Z in	Z out
3.6 MHz	1.5 V peak	10.09 V rms	9.49	-42 dB	24.8 kΩ	1.01 kΩ
7.1 MHz	0.8 V peak	8.08 V rms	14.2	-42 dB	13.5 kΩ	1.57 kΩ

R4 = 27 Ω	Input	Output	Av	F2	Z in	Z out
3.6 MHz	1.5 V peak	10.97 V rms	10.3	-42 dB	25.1kΩ	945Ω
7.1 MHz	0.8 V peak	9.08 V rms	15.9	-42 dB	13.9kΩ	1.49Ωk



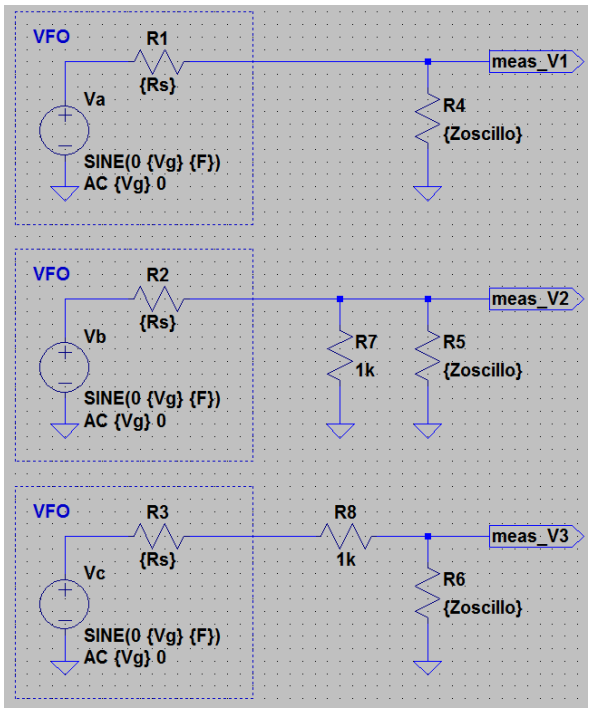
R1, R3, R4 to be changed

I cannot implement and test these modifications: both the VFO and buffer-amplifier have already been shipped to F6HOY. Anyhow it is better to do the final choice and tests when connected to the Viking transmitter.

Appendix – VFO output resistance estimate

F6HOY tests

The VFO output has been measured in three different configurations: direct measurement with no load, measurement with a shunt 1kΩ resistance and measurement with a series 1kΩ resistance. The VFO output impedance can be calculated by assuming that the VFO behaves as a Thevenin generator (i.e. a perfect fixed voltage source in series with a fixed output impedance). For simplification we consider that all impedances are resistive. The three configurations correspond to voltage dividers and their equations are:



$$I_1 = \frac{V_g}{R_s + Z_{oscillo}} = \frac{V_1}{Z_{oscillo}}$$

$$I_2 = \frac{V_g}{R_s + [Z_{oscillo}//R_{1k}]} = \frac{V_2}{[Z_{oscillo}//R_{1k}]}$$

$$I_3 = \frac{V_g}{R_s + R_{1k} + Z_{oscillo}} = \frac{V_3}{Z_{oscillo}}$$

$$[Z_{oscillo}//R_{1k}] = \frac{Z_{oscillo}\ R_{1k}}{Z_{oscillo} + R_{1k}}$$

After some manipulations, we obtain the following equations which allow calculating the VFO output impedance and its equivalent Thevenin tension as well as the oscilloscope input impedance:

$$0 = \left(\frac{V_1}{V_3} - 1\right)\left(\frac{R_s}{R_{1k}}\right)^2 - \left(\frac{R_s}{R_{1k}}\right) + \left(\frac{V_1}{V_2} - 1\right)$$

$$Z_{oscillo} = \frac{V_3}{V_{1-3}} R_{1k} - R_s$$

$$V_g = V_1\left(\frac{R_s}{Z_{oscillo}} + 1\right)$$

Note that these are purely theoretical calculations and that they might be way off the reality. The main reason is that they assume that the output impedance does not depends on the load. This is probably quite untrue for the VFO circuit.